Lecture 20

Photonic Packet Switching
Store-and-Forward Network

Figure 12.1 A generic store-and-forward network.
Routing Node

Figure 12.2  A routing node
Figure 12.3  (a) Function of a bit-interleaved optical multiplexer. (b) Function of a packet-interleaved optical multiplexer. The same four data streams are multiplexed in both cases. In (b), the packet size is shown as 3 bits for illustration purposes only; in practice, packets are much larger and vary in size. Note that the data must be compressed in time in both cases.
Figure 12.4 An optical multiplexer to create the bit-interleaved TDM stream shown in Figure 12.3(a). Only the operations at one node (node 3) are shown (after [Mid93, Chapter 6]).
Demultiplexing OTDM Signal

Figure 12.5  An optical demultiplexer to extract one of the multiplexed channels from a bit-interleaved TDM stream (after [Mid93, Chapter 6]).
Optical Packet-Interleaved TDM

Figure 12.6 An optical multiplexer to create a packet-interleaved TDM stream. (a) The packet passes through $k$ compression stages, where $2^k$ is the smallest power of two that is not smaller than the packet length $l$ in bits. (b) Detailed view of compression stage $j$ (after [SBP96]).
Optical Demultiplexing of Packet-Interleaved TDM Stream

Figure 12.7 An optical demultiplexer to extract one of the multiplexed channels from a packet-interleaved TDM stream.
Nonlinear Loop Mirror

Figure 12.8  (a) A nonlinear optical loop mirror. (b) A nonlinear amplifying loop mirror.
Asymmetric Demultiplexer

Figure 12.9  The terahertz optical asymmetric demultiplexer.
Soliton-Trapping AND Gate

Figure 12.10  Block diagram of a soliton-trapping logical AND gate.
Soliton Trapping

**Figure 12.11** Illustration of the operation of a soliton-trapping logical AND gate. (a) Only one pulse is present, and very little energy passes through to the filter output. This state corresponds to a logical zero. (b) Both pulses are present, undergo wavelength shifts due to the soliton-trapping phenomenon, and most of the energy from one pulse passes through to the filter output. This state corresponds to a logical one.
Synchronization

Figure 12.12  The function of a synchronizer. (a) The two periodic pulse streams with period $T$ are out of synchronization; the top stream is ahead by $\Delta T$. (b) The two periodic streams have been synchronized by introducing a delay $\Delta T$ in the top stream relative to the bottom stream.
Figure 12.13 A tunable delay line capable of realizing any delay from 0 to $T - T/2^{k-1}$, in steps of $T/2^{k-1}$. 
Feed-Forward Delay Line

Figure 12.14  Example of a 2 × 2 routing node using a feed-forward delay line architecture.
Output Buffering

Figure 12.15 A generic switch with output buffers.
Input Buffering

Figure 12.16  Head-of-line blocking in an input-buffered switch. Observe that the packet destined for output 1 in input buffer 2 is blocked despite the fact that the output is free.
Routing Node with Delay Lines

Figure 12.17 Example of a $2 \times 2$ routing node using a feedback delay line architecture.
Figure 12.18  An example of an output-buffered optical switch using fiber delay lines for buffers that does not use wavelengths for contention resolution.
Figure 12.19  An example of an output-buffered optical switch using multiple wavelengths internal to the switch and fiber delay lines for buffers. The switch uses tunable wavelength converters and arrayed waveguide gratings.
Figure 12.20  An example of an output-buffered optical switch capable of switching multiple input wavelengths. The switch uses TWGs and wavelength demultiplexers. The TWGs convert the input packets to the desired output wavelength, and the switch routes the packets to the correct output port and the appropriate delay line for that output.
### Comparison of Switch Architectures

Table 12.1  Number of delay lines required for different switch architectures. A uniformly distributed offered load of 0.8 per wavelength per input is assumed, with a packet loss probability of $10^{-6}$. The switch size is $16 \times 16$.

<table>
<thead>
<tr>
<th>Buffering Type</th>
<th>Input $\lambda$s</th>
<th>Internal $\lambda$s</th>
<th>Internal Fabric</th>
<th>Delay Lines per Output</th>
<th>Delay Lines Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output (Figure 12.18)</td>
<td>1</td>
<td>1</td>
<td>$16 \times 16$</td>
<td>25</td>
<td>400</td>
</tr>
<tr>
<td>Recirculating (Figure 12.17)</td>
<td>1</td>
<td>1</td>
<td>$23 \times 23$</td>
<td>7</td>
<td>112</td>
</tr>
<tr>
<td>Output (Figure 12.19)</td>
<td>1</td>
<td>64</td>
<td>$16 \times 16$</td>
<td>Shared</td>
<td>26</td>
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<tr>
<td>Output (Figure 12.20)</td>
<td>4</td>
<td>4</td>
<td>$64 \times 128$</td>
<td>7</td>
<td>112</td>
</tr>
<tr>
<td>Output (Figure 12.20)</td>
<td>8</td>
<td>8</td>
<td>$128 \times 80$</td>
<td>4</td>
<td>64</td>
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</tbody>
</table>
Don’t forget:
Home Work #2

Problem #12.3, with delay $xT/2^k$
(page 659 in the 2-nd edition book)
Provide general solution and consider a particular case with $k = 8$ and $x = 100$.
Note, $k$ stages would be required.

Due Nov. 27 before the class starts