**Hazards in a Pipeline Processor**

Pipeline is good but you need be careful.

**Pipelining: Its Natural!**

- Laundry Example
  - Ann, Brian, Cathy, Dave each have one load of clothes to wash, dry, and fold
  - Washer takes 30 minutes
  - Dryer takes 40 minutes
  - "Folder" takes 20 minutes

**Sequential Laundry**

<table>
<thead>
<tr>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 PM</td>
</tr>
<tr>
<td>30</td>
</tr>
</tbody>
</table>

Sequential laundry takes 6 hours for 4 loads

If they learned pipelining, how long would laundry take?

**Pipelined Laundry: Start work ASAP**

<table>
<thead>
<tr>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 PM</td>
</tr>
<tr>
<td>30</td>
</tr>
</tbody>
</table>

Pipelined laundry takes 3.5 hours for 4 loads

**Pipelining Lessons**

- Pipelining doesn't help latency of single task, it helps throughput of entire workload
- Pipeline rate limited by slowest pipeline stage
- Multiple tasks operating simultaneously
- Potential speedup = Number of pipe stages
- Unbalanced lengths of pipe stages reduces speedup
- Time to "fill" pipeline and time to "drain" it reduces speedup

**Why not pipeline for instructions?**
Review: Single Cycle, Multiple Cycle, vs. Pipeline

**Single Cycle Implementation:**
- Cycle 1: Load
- Cycle 2: Exec
- Cycle 3: Mem
- Cycle 4: Wr

**Multiple Cycle Implementation:**
- Cycle 1: Load
- Cycle 2: Ifetch
- Cycle 3: Reg
- Cycle 4: Exec
- Cycle 5: Mem
- Cycle 6: Wr
- Cycle 7: Ifetch
- Cycle 8: Reg
- Cycle 9: Exec
- Cycle 10: Mem
- Cycle 11: Wr

**Pipeline Implementation:**
- Load: Ifetch
- Load: Reg
- Load: Exec
- Load: Mem
- Load: Wr

Review: A Pipelined Datapath

**Pipeline Control “Data Stationary Control”**
- The Main Control generates the control signals during Reg/Dec
  - Control signals for Exec (ExtOp, ALUOp, ...) are used 1 cycle later
  - Control signals for Mem (Mem/Wr Branch) are used 2 cycles later
  - Control signals for Wr (MemtoReg Mem/Wr) are used 3 cycles later

**Pipeline Summary**
- Pipeline Processor:
  - Natural enhancement of the multiple clock cycle processor
  - Each functional unit can only be used once per instruction
  - If a instruction is going to use a functional unit:
    - it must use it at the same stage as all other instructions
- Pipeline Control:
  - Each stage’s control signal depends ONLY on the instruction that is currently in that stage

**Limits to pipelining:** Hazards prevent next instruction from executing during its designated clock cycle
- Structural hazards (hardware resource conflicts): HW cannot support this combination of instructions (single person to fold and put clothes away)
- Data hazards (data dependencies): Instruction depends on result of prior instruction still in the pipeline (missing sock)
- Control hazards (changes in program flow): Pipelining of branches & other instructions “pops” the pipeline until the hazard (“bubbles”) in the pipeline disappear.

**Single Memory is a Structural Hazard**

**Hazards = Such Hazardous events**
Option 1: Stall to resolve Memory Structural Hazard

Time (clock cycles)

Instr 1
Instr 2
Instr 3 (stall)
Instr 4

Load
Mem
Reg

Option 2: Duplicate to Resolve Structural Hazard

Time (clock cycles)

Instr 1
Instr 2
Instr 3
Instr 4

Load
Im
Reg

Separate Instruction Cache (Im) & Data Cache (Dm)

Data Hazard on r1

add r1, r2, r3
sub r4, r1, r3
and r6, r1, r7
or r8, r1, r9
xor r10, r1, r11

Dependencies backwards in time are hazards

Shading on right/left half means read/write on that element.

Option 1: HW Stalls to Resolve Data Hazard

Time (clock cycles)

add r1, r2, r3
sub r4, r1, r3
and r6, r1, r7
or r8, r1, r9
xor r10, r1, r11

• The Control logic can be complex

But recall use of “Data Stationary Control”

• The Main Control generates the control signals during Reg/Dec
  • Control signals for Exec (ExtOp, ALUSrc, ...) are used 1 cycle later
  • Control signals for Mem (MemWr Branch) are used 2 cycles later
  • Control signals for Wr (MemtoReg MemWr) are used 3 cycles later
Option 1: How HW really stalls pipeline

- HW doesn’t change PC stays fetching same instruction & sets control signals to benign values (0)

Time (clock cycles)

```
add r1, r2, r3  
stall  
stall  
sub r4, r1, r3  
and r6, r1, r7
```

Option 2: SW inserts independent instructions

- Worst case inserts NOP instructions

Time (clock cycles)

```
add r1, r2, r3  
nop  
nop  
nop  
sub r4, r1, r3  
and r6, r1, r7
```

Option 3 Insight: Data is available!

- Pipeline registers already contain needed data

Time (clock cycles)

```
add r1, r2, r3  
sub r4, r1, r3  
and r6, r1, r7  
or r8, r1, r9  
xor r10, r1, r11
```

HW Change for “Forwarding” (Bypassing):

- Increase multiplexors to add paths from pipeline registers
- Assumes register read during write gets new value (otherwise more results to be forwarded)

From Last Lecture: The Delay Load Phenomenon

- Although Load is fetched during Cycle 1:
  - The data is NOT written into the Reg File until the end of Cycle 5
  - We cannot read this value from the Reg File until Cycle 6
  - 3-instruction delay before the load take effect

Forwarding reduces Data Hazard to 1 cycle:

Time (clock cycles)

```
lw r1, 0(r2)  
sub r4, r1, r6  
and r6, r1, r7  
or r8, r1, r9
```
Option 1: HW Stalls to Resolve Data Hazard

- "Interlock": checks for hazard & stalls

Try producing fast code for
\[ a = b + c; \]
\[ d = e – f; \]
assuming a, b, c, d, e, and f in memory.

Slow code:
- LW Rb, b
- LW Rc, c
- ADD Ra, Rb, Rc
- SW a, Ra
- LW Rf, f
- SW d, Rd

Fast code:
- LW Rb, b
- LW Rc, c
- ADD Ra, Rb, Rc
- LW Rf, f
- SW a, Ra
- SW d, Rd

Software Scheduling to Avoid Load Hazards

Try producing fast code for
\[ a = b + c; \]
\[ d = e – f; \]
assuming a, b, c, d, e, and f in memory.

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- LW Rf, f
- SW d, Rd

Fast code:
- LW Rb, b
- LW Rc, c
- ADD Ra, Rb, Rc
- LW Rf, f
- SW a, Ra
- SW d, Rd

Compiler Avoiding Load Stalls:

<table>
<thead>
<tr>
<th>Program</th>
<th>scheduled</th>
<th>unscheduled</th>
</tr>
</thead>
<tbody>
<tr>
<td>gcc</td>
<td>11%</td>
<td>54%</td>
</tr>
<tr>
<td>spice</td>
<td>14%</td>
<td>42%</td>
</tr>
<tr>
<td>tex</td>
<td>25%</td>
<td>65%</td>
</tr>
</tbody>
</table>

% loads stalling pipeline

From Last Lecture: The Delay Branch Phenomenon

1. Although Beq is fetched during Cycle 4:
   - Target address is NOT written into the PC until the end of Cycle 7
   - Branch's target is NOT fetched until Cycle 8
   - 3-instruction delay before the branch take effect
Branch Stall Impact

- If CPI = 1, 30% branch, Stall 3 cycles \( \Rightarrow \) new CPI = 1.9
- 2 part solution:
  - Determine branch taken or not sooner, AND
  - Compute taken branch address earlier
- MIPS branch tests = 0 or \( \neq 0 \)
- Solution Option 1:
  - Move Zero test to ID/RF stage
  - Adder to calculate new PC in ID/RF stage
  - 1 clock cycle penalty for branch vs. 3

Option 1: move HW forward to reduce branch delay

Option 2: Define Branch as Delayed

Branch Delay now 1 clock cycle

When is pipelining hard? (1)

- Interrupts: 5 instructions executing in 5 stage pipeline
  - How to stop the pipeline?
  - Restart?
  - Who caused the interrupt?

When is pipelining hard? (2)

- Complex Addressing Modes and Instructions
  - Address modes: Auto increment causes register change during instruction execution
    - Interrupts?
    - Now worry about write hazards since write no longer last stage
    - Write After Read (WAR): Write occurs before independent read
    - Write After Write (WAW): Writes occur in wrong order, leaving wrong result in registers
    - (Previous data hazard called RAW, for Read After Write)
  - Memory-memory Move instructions
    - Multiple page faults
    - make progress?
When is pipelining hard? (3)

° Floating Point: long execution time
° Also, may pipeline FP execution unit so that can initiate new instructions without waiting full latency

<table>
<thead>
<tr>
<th>FP Instruction</th>
<th>Latency</th>
<th>Initiation Rate (MIPS R4000)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add, Subtract</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>Multiply</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>Divide</td>
<td>36</td>
<td>35</td>
</tr>
<tr>
<td>Square root</td>
<td>112</td>
<td>111</td>
</tr>
<tr>
<td>Negate</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Absolute value</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>FP compare</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

° Divide, Square Root take -10X to -30X longer than Add
  - Exceptions?
  - Adds WAR and WAW hazards since pipelines are no longer same length

Data Hazards

° Read After Write (RAW):
  - Attempting to read a value that hasn't been written yet. This is the most common type, and can be overcome by forwarding.
° Write after write (WAW):
  - Writing a value before a preceding write has completed. This can only happen in complex pipes that allow instructions to proceed out of order, or that have multiple write-back stages (mostly CISC), or that have multiple pipes that can write.
° Write after read (WAR):
  - Writing a value before a preceding read has completed. These also require a complex pipeline that can sometimes write in an early stage, and read in a later stage. It is also possible when multiple pipelines or out-of-order issue are employed.
° Read after read (RAR) does not produce a hazard.

Hazard Detection

Suppose instruction \( i \) is about to be issued and a predecessor instruction \( j \) is in the instruction pipeline.

\[ \text{Regs}(i) = \text{Registers read by instruction } i \]

\[ \text{Wregs}(i) = \text{Registers written by instruction } i \]

° A RAW hazard exists on register \( p \) if \( p \in \text{Regs}(i) \cap \text{Wregs}(j) \)
  - Keep a record of pending writes (for inst's in the pipe) and compare with operand regs of current instruction.
  - When instruction issues, reserve its result register.
  - When one operation completes, remove its write reservation.

° A WAW hazard exists on register \( p \) if \( p \in \text{Wregs}(i) \cap \text{Wregs}(j) \)

° A WAR hazard exists on register \( p \) if \( p \in \text{Wregs}(i) \cap \text{Rregs}(j) \)

Avoiding Data Hazards by Design

Suppose instructions are executed in a pipelined fashion such that instructions are initiated in order.

° WAW avoidance: if writes to a particular resource (e.g., reg) are performed in the same stage for all instructions, then no WAW hazards occur.
  - proof: writes are in the same time sequence as instructions.

\[
\begin{array}{cccc}
I & R & D & E \\
I & R & D & W \\
I & R & Q & E \\
I & R & Q & W
\end{array}
\]

° WAR avoidance: if in all instructions reads of a resource occur at an earlier stage than writes to that resource occur in any instruction, then no WAR hazards occur.
  - proof: A successor instruction must issue later, hence it will perform writes only after all reads for the current instruction.

First Generation RISC Pipelines

° All instructions follow same pipeline order ("static schedule").
° Register write in last stage
  - Avoid WAW hazards
° All register reads performed in first stage after issue.
  - Avoid WAR hazards
° Memory access in stage 4
  - Avoid all memory hazards
° Control hazards resolved by delayed branch (with fast path)
° RAW hazards resolved by bypass, except on load results which are resolved by flat (delayed load).

Substantial pipelining with very little cost or complexity.
Machine organization is (slightly) exposed!
Relies very heavily on "hit assumption" of memory accesses in cache

Review: Summary of Pipelining Basics

° Speed Up \( \frac{\text{Pipeline Depth}}{\text{CPI}} \); if ideal CPI is 1, then:

\[ \text{Speedup} = \frac{\text{Pipeline depth}}{\text{Clock cycle unpipelined}} \times \frac{\text{Clock cycle pipelined}}{\text{Clock cycle unpipelined}} \]

° Hazards limit performance on computers:
  - structural: need more HW resources
  - data: need forwarding, compiler scheduling
  - control: early evaluation & PC, delayed branch, prediction

° Increasing length of pipe increases impact of hazards since pipelining helps instruction bandwidth, not latency

° Compilers key to reducing cost of data and control hazards
  - load delay slots
  - branch delay slots

° Exceptions, Instruction Set, FP makes pipelining harder

° Longer pipelines => Branch prediction, more instruction parallelism?