A Microprocessor-Based Switched-Battery Capacitance Meter

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Abstract—A microprocessor-based, switched-battery capacitance meter has been developed. It consists of an analog part, based on a previously designed capacitance meter [2], and a digital part in which a microprocessor and a timer perform the main functions. The capacitance is measured indirectly by means of the time constant measurement. Two phases of the measurement process are involved for measuring the capacitance. The first phase, when a capacitor is charged, is based on the software counter-timer measurements. The second phase, when the capacitor is discharged, requires a hardware timer controlled by the microprocessor. The hardware presented in this paper shows a different approach to the digital part of the previous construction.

I. INTRODUCTION

SEVERAL PAPERS have been published on digital capacitance meters [1]–[3]. This paper presents an improved version of a switched-battery digital capacitance meter described in [2]. The measurement cycle of the meter presented in [2] has two main phases: a charging phase and a discharging phase. In the charging phase, first the capacitor is charged to half of the battery voltage level, and this part of the charging phase time (Tc) is measured by a 24-bit binary counter. The capacitor is then charged for the time T2 = M * T1, where M = 255, which is large enough to ensure that the capacitor is charged to almost the battery voltage. The lower bound on the value of M is computed in Appendix I. In the discharging phase, when the battery polarities are reversed, the time (Td) required to discharge the capacitor from the battery voltage level to the zero level is also measured by the same 24-bit counter. This time, which is proportional to the value of the capacitance, is registered and displayed by the meter. The digital part of the meter, which consists of about 20 integrated circuits, could be replaced by an integrated timer, controlled by a microprocessor.

II. PRINCIPLES OF OPERATION OF THE MICROPROCESSOR-BASED, SWITCHED-BATTERY CAPACITANCE METER

The meter has two main parts: the analog part directly incorporated from the meter described in [2] and the new digital part with an 8254 integrated timer and a 6809E microprocessor, supported by several gates and flip-flops.

The implementation of the new digital part is shown in Fig. 1. Lines with signals X, Y, and Z serve as the communication links between the digital and analog parts of the meter. Signal X is applied to the analog part from the digital part, and it is used to initiate the charging and discharging phases of the meter. Signals Y and Z are delivered to the digital part from the analog part. The 8254 timer [4] has three 16-bit counters and a control word register. One of the three counters or the control word register is selected by sending proper signals through lines A0 and A1 of the timer. The select logic is shown in Fig. 2. Since the timer circuit does not have any software-controlled peripheral I/O lines, signal X is generated by using a J = K flip-flop (FF-2) and decoding the signals on the pins RD, A0, A1, and CS of the timer. As indicated in Fig. 1, X is made high by reading Counter-1 and it is made low by reading the control word register. Similarly, flip-flop 1 (FF-1) is set to 1 by reading Counter-2. It should be noted that a read operation does not affect the operation of any counter. As shown in Fig. 1, the 8254 timer is clocked by an external clock. Since this external clock also controls signal X, it doesn’t have to be synchronized with the 6809E clock.

When power is turned on, both the digital and analog parts of the meter are initialized. This makes the initial values of signals X and Y low, and signal Z high, as shown in Fig. 3. Flip-flop 1 is also set at initialization. Since the measurements of T1 and T2 do not have to be very accurate as long as the ratio T2/T1 is high, a software counter is used to measure these two times. The computation of the minimum ratio of T2/T1 is shown in Appendix I.

The microprocessor starts the operation of the meter by making signal X high, and starting a software counter to measure T1. A low-to-high transition of X initiates the charging phase of the meter. As soon as the capacitor is charged to one-half of the battery voltage, the signal Z, as shown in Fig. 3, becomes low. As a result, FF-1 is clocked low and the microprocessor is interrupted through the IRQ line. At this time the microprocessor reads T1 from the software counter and sets FF-1 to 1. The microprocessor then resets and starts the software counter again, and the counter keeps on counting until the count becomes T2 = M * T1.

The charging phase of the meter ends after the software count becomes equal to T2. At this time the microprocessor first writes the control word to select Counter-0 under Mode-2 (rate generator) operation of the 8254 timer, and

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then it writes the maximum count \(2^{16}\) into Counter-0. After this step, the microprocessor clears FF-2 by reading the control word register. As soon as FF-2 is cleared, signal X changes to a low level and the GATE-0 input of the

8254 timer becomes high. A high-to-low transition of signal X reverses the polarities of the battery. This reversal initiates the discharging phase of the meter. A low-to-high transition on the GATE-0 input initiates Counter-0 to count down. Counter-0 begins decrementing by one at every CLOCK-0 pulse starting from the next CLOCK-0 pulse after GATE-0 changes to high level. In Mode-2 operation, when Counter-0 is decremented to 1, a negative pulse is sent from the OUT-0 line, the counter is reloaded with the initial count \(2^{16}\) automatically, and the process is repeated. At the negative edge of the OUT-0 pulse the microprocessor is interrupted so that the microprocessor can increment another software counter by 1 to figure out the number of times the signal OUT-0 went low. In this case, signal OUT-0, as shown in Fig. 4, remains at a low level for only one CLOCK-0 cycle. If the microprocessor is to be interrupted by the NMI line, then this interrupt line must go low and remain at a low level for at least one 6809E clock cycle. Hence, OUT-0 cannot be connected directly to the NMI line to interrupt the microprocessor, because the ratio of the CLOCK-0 frequency to the 6809E clock frequency could be as high as 10. Thus, Counter-1 is used under Mode-1 of the 8254 timer (hardware retriggerable one-shot) to generate a wide negative pulse on the OUT-1 line as soon as OUT-0 reaches a low level. In Mode-1, Counter-1 is loaded from its count register as soon as there is a low-to-high transition on the GATE-1 input line. The OUT-1 line goes low one CLOCK-1 cycle after the rising edge of the GATE-1 signal, and it remains at low level for \(K\) cycles, where \(K\) is the content of the count register of Counter-1. If \(K\) is greater than the ratio of the CLOCK-1 frequency to the 6809E clock frequency, then the microprocessor can be interrupted by connecting the OUT-1 line directly to the NMI line of the microprocessor. The count register of Counter-1 is loaded with \(K\) at the time the system is initialized.

As shown in Fig. 3, the analog part again interrupts the microprocessor through the IRQ line, as soon as the capacitor voltage reaches the zero level, i.e., when \(Y\) goes low. As soon as \(Y\) changes to a low level, the signal GATE-0 becomes low, and it disables Counter-0, i.e., Counter-0 stops decrementing. The microprocessor then reads the contents of Counter-0. Let this count be \(t_d\). The microprocessor then computes time \(T_d\) as follows:

\[
T_d = \left[ N \cdot (2^{16} - 1) + (2^{16} - t_d) + 1 \right] \cdot T
\]  

where \(N\) is the number of times Counter-0 was reloaded, i.e., the number of times the microprocessor was interrupted by the NMI line, and \(T\) is the period of the clock connected to the 8254 timer. Since Counter-0 starts counting one clock cycle after GATE-0 signal becomes high, the term +1 appears in (1). The count \(T_d\) is proportional to the value of the capacitance, which is expressed below

\[
C = \frac{T_d}{R \cdot \ln 2}
\]

where \(R\) is the resistance of the charging circuit.
The process steps in the meter are given in the flow diagram in Fig. 5(a) and (b).

III. ERROR SOURCES AND EXPERIMENTAL RESULTS

The analog part of the meter is the same as the one used in [2]. Hence, the error analysis for the errors due to the analog part is exactly the same as that described in [2]. Error in the digital part is associated mainly with the measurement of time $T_d$. This error depends on the frequency of the clock used to run the 8254 timer. The high-speed version of the 8254 timer can handle clock inputs up to 10 MHz. Thus, the maximum error associated with $T_d$ could be about 100 ns which corresponds to 0.14 pF for $R_A = 1 \text{ M} \Omega$.

Table I summarizes information pertaining to the error sources of the capacitance meter.

Experimental results were concerned with testing the main waveforms of the digital part. The timing diagrams of Figs. 3 and 4 were verified by the experimental results. Experimental results showed that the performance of this meter is as good as that of the meter described in [2].

IV. CONCLUSION

A microprocessor-based, switched-battery capacitance meter has been designed and tested. The design requires fewer integrated circuits than applied in [2], and the suggested microprocessor could also be used within the same instrument to perform additional functions like averaging and autoranging, or it could control other instruments. The microprocessor controls the operation of the timer and the analog part of the meter developed in [2]. Thus, most of the design efforts have been transferred to software development. The results show that the overall microprocessor-based meter performance is limited basically by the same factors as the digital meter published in [2], but for the same clock (external) frequency it is more accurate, and it could also be more versatile.
The voltage across the capacitor during the charging phase can be expressed as

\[ v = v_2 + (v_1 - v_2) * e^{-t/RC} \]  \hspace{1cm} (A-1)

where, \( v_1 \) is the voltage across the capacitor at the beginning of the charging phase, i.e., at \( t = 0 \), and \( v_2 \) is the battery voltage (see Fig. 3). The value of \( v_2 \) can be in the range \(-v_2 \leq v_1 \leq 0\), depending upon the final conditions of the previous measurement cycle. The voltage \( v_{T2} \) across the capacitor at time \( t = T2 + T1 \) can be expressed as

\[ v_{T2} = v_2 + (v_1 - v_2) * e^{-(T2 + T1)/RC} \]  \hspace{1cm} (A-2)

From (A-2)

\[ T2 + T1 = RC \ln \left( \frac{(v_2 - v_1)}{(v_2 - v_{T2})} \right) \] \hspace{1cm} (A-3)

Similarly if \( v_{T1} \) is the voltage at time \( t = T1 \), then \( T1 \) can be expressed as

\[ T1 = RC \ln \left( \frac{(v_2 - v_1)}{(v_2 - v_{T1})} \right) \] \hspace{1cm} (A-4)

Since \( T1 \) is the time required to charge the capacitor up to half of the battery voltage, \( v_{T1} = v_2/2 \), and from (A-4)

\[ T1 = RC \ln \left( \frac{2(v_2 - v_1)}{v_2} \right) \] \hspace{1cm} (A-5)

Now from (A-3) and (A-5) the ratio \( T2/T1 \) can be written as

\[ \frac{T2}{T1} = \ln \left( \frac{(v_2 - v_1)}{(v_2 - v_{T2})} \right) \cdot \ln \left( \frac{2(v_2 - v_1)}{v_2} \right) - 1 \] \hspace{1cm} (A-6)

Let \( v_2 - v_1 = k * v_2 \) and \( v_2 - v_{T2} = e * v_2 \). Then (A-6) becomes

\[ \frac{T2}{T1} = \ln \left( \frac{k}{e} \right) \ln (2k) - 1 \] \hspace{1cm} (A-7)

Equation (A-7) shows that the ratio \( T2/T1 = 0 \) when \( e = 0.5 \). If \( e > 0.5 \) the ratio decreases as the value of \( k \) decreases, but if \( e < 0.5 \) the ratio increases as the value of \( k \) decreases. Since the value of \( v_1 \) is in the range \(-v_2 \leq v_1 \leq 0\), the value of \( k \) is in the range \( 1 \leq k \leq 2 \). During the charging phase it is desired to charge the capacitor almost up to the battery voltage, that means \( v_{T2} \equiv v_2 \), which means \( e \equiv 0 \). Since \( e < 0.5 \) and the range of \( k \) is \( 1 \leq k \leq 2 \), the ratio \( T2/T1 \) will be maximum for \( k = 1 \), and the maximum value of \( T2/T1 \), for a given value of \( e \), can be expressed as

\[ \left( \frac{T2}{T1} \right)_{\text{max}} = \ln \left( \frac{1}{e} \right) \ln (2) - 1 \] \hspace{1cm} (A-8)

This is the lower bound of the ratio \( M = T2/T1 \) which must be used in the capacitance meter to ensure that the capacitor will be charged up to the desired voltage during the charging phase. For \( v_{T2} \) to be equal to 0.99999 \( v_2 \), i.e., for \( e = 0.0001 \), the minimum value of \( M \) has to be equal to 12.29. A value of \( M = 255 \) was used in the meter presented in this paper.

References


