Effective learning requires reading the textbook, attending classes, looking at my class materials, adding your own notes to the class materials, doing large amount of exercises.

ECE 4680 Final Exam

I have neither given nor received unauthorized assistance on this exam.

Signed: _______________________ Date: _____________________

Do not open without the permission from instructor.

Read the following rules before you start to answer:

This test is open-book and open-notes.

1) You may use calculator.
2) You are allowed 110 minutes from 5:30PM to 7:20PM.
3) Write your answer on the bluebook. No scratch papers are provided.
4) Do not ask any questions during the whole examination.

Wayne State University

April 23, 2003
Today’s Review is more for what we have discussed than for the final examination.
Chapter 5 Single-cycle Datapath and Control

- 7 typical instructions
- What is datapath?
  - ALU, Adder, Gates, MUX, Memory, Decoder, Registers: Which are operational elements? Which are state elements?
  - Connections: bus, link, control signals.
  - Longest path: load instruction
- What is control?
  - Controller: How to generate control signals?
  - Where to go? To Gate, to MUX, or to ALU?
    Only ALUctr to ALU, only MemWr and RegWr to AND gate.
  - The purpose of each control signal: When, where and for what instruction is it set?
- Given each instruction, what is the single-cycle datapath?
- Given each instruction, what is the single-cycle control?
- Given each control signal, what instructions will need it?

Chapter 5 Multiple-cycle Datapath (continue)

- Comparison of single-cycle and multiple-cycle
- Timing of 5-stage load instruction
- How to determine the cycle length? Longest length vs. longest stage.
- A unit can be used multiple times for one instruction, e.g. memory and ALU. As a result, there is only one ALU without next address logic, and only one Memory
- Race condition of address and write enable, and 2 solutions.
- Multiple cycle delay path: what is the necessary conditions? Advantages?
- Given each instruction, how many cycles, what control signals are required?
Chapter 6  Pipeline

- Why we need pipeline?
- Why do we say that pipeline processor is more like 1-cycle processor?
- What are the 2 conditions for ideal pipeline with conflict?
- How to compute the speedup if given limited number of instructions?
- Datapath and control for pipeline processor.
- 3 types of pipeline hazards: structural, data, and control
- 4 types of data dependency but only 3 types of data hazard.
- Solutions:
  - For structural: stall, duplicate
  - For data: stall, nop, forwarding
  - For control, stall, nop, forwarding, insert
- How to compute CPI under stalled cases?
- How to readjust program order to reduce the hazard.

Chapter 7  Memory

- Why hierarchical?
- 2 types of locality: examples in program.
- 2 objectives: as fast as top level; as large as bottom level.
- \[ \text{Average Access Time} = \text{Hit Time} \times (1 - \text{Miss Rate}) + \text{Miss Penalty} \times \text{Miss Rate} \]
- Cache design
  - Objective: decrease hit time, miss penalty and miss rate
  - 3 types of cache: directly mapped, fully associate, set-associative
  - Relationship between Block size and locality
  - Pros and cons: how to measure the cost?
  - Set-associate is the combination of the former 2 types.
  - Replacement: Random, FIFO, LRU, LFU.
  - Under different policy, how to calculate hits and misses?
- Virtual memory
  - Paging organization and segmentation
  - Page table, TLB