Problem-1 (16 Points)
Write a few instructions to program the pulse accumulator as follows:

- Enable the pulse accumulator.
- Select the event counting mode.
- Select the rising edge of PAI line to count.
- Keep checking the pulse accumulator to determine when it overflows.
- Increment the byte at location $0210$ by 5, every time you detect an overflow on the pulse accumulator.

```
BSET PACTL,X $50          Set PAEN and PEDGE
BCLR PACTL,X $A0          Clear DDRA7 and PAMOD
LOOP BCLR TFLG2,X $DF     Clear PAOVF
WAIT BRCLR TFLG2,X $20    Wait until PAOVF is set
LDA A 
ADD $0210 A = A + Content of location $0210
STAA $0210 Store A in to location $0210
BRA LOOP Repeat
```

Problem-2 (16 Points)
Write a few instructions to check the input lines PA0, PA1 and PA2, and then send a signal through the output line PA5.
If PA0=0, PA1=1 and PA2=0 then make PA5=1. Otherwise, make PA5=0.

```
LOOP BRCLR PORTA,X 5 NEXT Go to NEXT if PA0=0 and PA2=0
CLEAR BCLR PORTA,X $20   PA5=0
       BRA LOOP             Repeat
       NEXT BRCLR PORTA,X 2 CLEAR Go to CLEAR if PA1=0
BSET PORTA,X $20          PA5=1
       BRA LOOP             Repeat
```

Problem-3 (16 Points)
Write a few instructions to do the following

- Wait until there is a match between TCNT and TOC4 registers.
- When there is a match between TCNT and TOC4 registers, increment the byte at location $0220$ by 10.

```
WAIT     BRCLR     TFLG1,X $10     WAIT     Wait until OC2F is set
         LDAA       #10     A = 10
         ADDA       $0220   A = A + Content of location $0220
         STAA       $0220   Store A into location $0220
```

**Problem-4 (16 Points)**
Write a few instructions to do the following

- Enable IC1 and IC3 interrupts.
- Program IC1 to capture a falling edge, and IC3 to capture a rising edge.

```
TMSK1    $1022
  7  6  5  4  3  2  1  0
  OC1I OC2I OC3I OC4I OC5I IC1I IC2I IC3I

TCTL2    $1021
  7  6  5  4  3  2  1  0
  EDG1B EDG1A EDG2B EDG2A EDG3B EDG3A

BSET     TMSK1,X 5     Set IC1I and IC3I
BSET     TCTL2,X $21   Set EDG1B and EDG3A
BCLR     TCTL2,X $12   Clear EDG1A and EDG3B
```

**Problem-5 (16 Points)**
The following OC2 interrupt service routine has been written for a system with a 1MHz clock and a timer pre-scale factor equal to four.

A. If the OC2 interrupt is enabled, then how often the processor will go to the subroutine TASK.

B. Show the necessary changes that you have to make in the following code, if we want to run the code in a system with a 2 MHz clock and a timer pre-scale factor equal to two. In both systems the processors must go to the TASK routine the same number of times per sec.

```
TIME     EQU     8192
*---------------------------------------------------------------------------
OC2SERV  LDD     TOC2,X ; Read TOC2 and then
         ADDD    #TIME
         STD     TOC2,X ; Update TOC2 for the next interrupt
         JSR     TASK
         RTI
```
Since the timer pre-scale factor is four, the frequency of the timer clock is \(1\text{MHz}/4 = 250\text{KHz}\). Hence, the timer will go up by one once every \(1/250\text{KHz} = 4\ \text{microsec}\).

Thus, a period of 8192 counts is equivalent to \(8192\times4 = 32768\ \text{microsec} = 32.768\ \text{msec}\).

The frequency of the timer clock for a system with \(E=2\text{MHz}\) and pre-scale factor equal to two, is \(2\text{MHz}/2 = 1\text{MHz}\). Hence, the timer will go up by one once every \(1/1\text{MHz} = 1\ \text{microsec}\).

Thus 32768 counts will give a delay of 32768 microsec = 32.768 msec.

Hence, the following change is the only change that we will see in the program.

\[
\text{TIME EQU 32768}
\]

**Problem-6 (10 Points)**

Determine the bit pattern that you have to store in register ADCTL to configure the A/D converter as follows:

- Select non-scan mode.
- Select single channel mode.
- Select channel number 4.

<table>
<thead>
<tr>
<th>ADCTL</th>
<th>$1030</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

CCF --- SCAN MULT CD CC CB CA

**Problem-7 (10 Points)**

The frequency of E clock is 4 MHz. Assume that the pulse accumulator starts counting in gated accumulation mode. How often will the pulse accumulator overflow if we let the counter keep counting continuously?

The frequency of the Pulse Accumulator Clock is \(4\text{MHz}/64 = 62.5\ \text{KHz}\)

Hence, the Pulse Accumulator will go up by one once every \(1/62.5\text{KHz} = 16\ \text{microsec}\).

Since the Pulse Accumulator is an 8-bit counter it will overflow once every \(256\times16 = 4096\ \text{microsec} = 4.096\ \text{msec}\).